

# CMOS Transistor Array

For Linear Circuit Applications

**Features:**

- High input resistance . . . . . 100 GΩ (typ.)
- Low gate-terminal current . . . . . 10 pA (typ.)
- Matched p-channel pair:
  - Gate-voltage differential ( $I_D = -100 \mu A$ )  $\pm 20$  mV (max.)
- No "Popcorn" (burst) noise
- Stable transfer characteristics over an operating temperature range of  $-55^\circ C$  to  $+125^\circ C$  when operated in complementary circuit configuration at supply voltages in the 5 to 15 volt range (see Fig. 14)
- Integrated integral gate-protection system (see Fig. 34)
- High voltage gain (see Fig. 11). . . up to 53 dB (typ.) per CMOS stage
- Individual MOS transistors have square-law characteristics, superior cross-modulation performance, and greater dynamic range than bipolar transistors

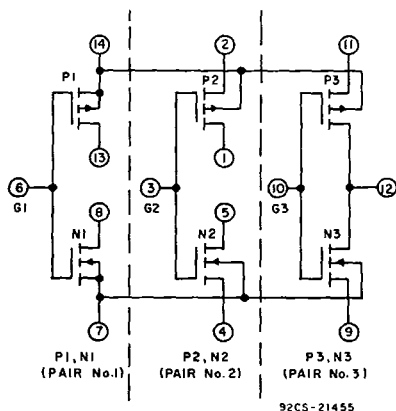
RCA-CA3600E is an array of Complementary-Symmetry MOS Field-Effect Transistors\* on a monolithic silicon substrate. It is comprised of three n-channel and three p-channel enhancement-type MOS transistors arrayed as shown in Fig. 1, and specified and tested for linear circuit operation. These transistors are uniquely suitable for service in complementary-symmetry circuits at supply voltages in the range of 3 to 15 volts and are useful at frequencies up to 5 MHz (untuned). Each transistor in the CA3600E can conduct currents up to 10 mA. This device is supplied in the 14-lead dual-in-line plastic package.

Formerly RCA Dev. No. TA6368.

\* The theory and construction of COS/MOS transistors are described in the "RCA CMOS Integrated Circuits Manual," RCA Solid State Division Technical Series Publication No. CMS-272.

**Applications:**

- High input impedance, general-purpose amplifiers
- Pre-amplifiers
- Differential amplifiers
- Op-amps and comparators
- Constant-current sources and current mirrors
- Micropower amplifiers and oscillators
- Control of lamps, LED's, relays, and thyristors
- Timers
- Choppers
- Mixers



1. Drain terminal, p-channel of pair no. 2
2. Source terminal, p-channel of pair no. 2
3. Common gate terminal of pair no. 2
4. Source terminal, n-channel of pair no. 2
5. Drain terminal, n-channel of pair no. 2
6. Common gate terminal of pair no. 1
7. Source terminal, n-channel of pair no. 1 and substrate connection for all n-channel transistors . . . V<sub>SS</sub> terminal
8. Drain terminal, n-channel of pair no. 1
9. Source terminal, n-channel of pair no. 3
10. Common gate terminal of pair no. 3
11. Source terminal, p-channel of pair no. 3
12. Common drain terminal of pair no. 3
13. Drain terminal, p-channel of pair no. 1
14. Source terminal, p-channel of pair no. 1 and substrate connection for all p-channel transistors . . . V<sub>DD</sub> terminal

Fig. 1 — Schematic diagram for CA3600E CMOS transistor array. (See Fig. 34 for internal gate-and-channel-protection circuits)

Terminal Identification for Fig. 1.

# CA3600

## MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

### DISSIPATION:

Any one transistor at $T_A$ up to $55^\circ\text{C}$ . . . . .	150 mW
Total package at $T_A$ up to $55^\circ\text{C}$ . . . . .	750 mW
Above $T_A = 55^\circ\text{C}$ . . . . .	derate linearly 6.67 mW/ $^\circ\text{C}$

### AMBIENT TEMPERATURE RANGE:

Operating . . . . .	$-55$ to $+125^\circ\text{C}$
Storage . . . . .	$-65$ to $+150^\circ\text{C}$

### LEAD TEMPERATURE (During Soldering)

At distance not less than $1/16'' \pm 1/32''$ ( $1.59 \pm 0.79$ mm) from case for 10 s max. . . . .	$265^\circ\text{C}$
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### The Following Ratings Apply for Each Transistor in the Device:

#### DRAIN-TO-SOURCE VOLTAGE, $V_{DS}$ :

n-channel . . . . .	+15 V
p-channel . . . . .	-15 V

#### DRAIN-TO-GATE VOLTAGE, $V_{DG}$ :

n-channel . . . . .	+15 V
p-channel . . . . .	-15 V

#### SOURCE-TO-SUBSTRATE VOLTAGE, $V_{SB}$ :

n-channel . . . . .	+15 V
p-channel . . . . .	-15 V

#### GATE-TO-SOURCE VOLTAGE, $V_{GS}$ :

p-channel transistors ( $p_1, p_2, p_3$ ). . . . .	$0$ V(min.), $-V_D$ (max.)
n-channel transistors ( $n_1, n_2, n_3$ ). . . . .	$0$ V(min.), $+V_D$ (max.)
CMOS transistor-pairs ( $p_1$ - $n_1, p_2$ - $n_2, p_3$ - $n_3$ ). . . . .	$0$ V(min.), $+V_{DD}$ (max.)

DRAIN CURRENT, $ I_D $ . . . . .	10 mA
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GATE CURRENT, $ I_G $ . . . . .	100 $\mu\text{A}$
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### The Following Rating Applies for Each CMOS Transistor-Pair in the Device:

DC SUPPLY VOLTAGE ( $V_{DD} - V_{SS}$ ) . . . . .	+ 15 V
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### Rules for Maintaining Electrical Isolation Between Transistors and Monolithic Substrate

Terminal No. 14 must be maintained at the most positive potential (or equally positive potential) with respect to any other terminal in the CA3600E.

Terminal No. 7 must be maintained at the most negative potential (or equally negative potential) with respect to any other terminal in the CA3600E.

Violation of these rules will result in improper transistor operation, circuit "latching" and/or possible permanent damage to the CA3600E.

Note: Users should observe the "Considerations in Handling CA3600E Devices", discussed on page 13.

# CA3600

## ELECTRICAL CHARACTERISTICS, At $T_A = 25^{\circ}\text{C}$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
<b>For Each p-Channel MOS Transistor</b>							
Drain Current	$I_D$	$V_{DS} = -10\text{ V}, V_{GS} = -3.6\text{ V}$	2,3,4	-0.5	-1.1	-2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	$I_D = -10\text{ }\mu\text{A}$	-	-	-1.75	-	V
Gate-to-Source Voltage Differential ( $p_1$ vs. $p_2$ )	$ V_{GS1} - V_{GS2} $	$I_D = -100\text{ }\mu\text{A}, V_{DS} = -10\text{ V}$	5	-	$\pm 4$	$\pm 20$	mV
Forward Transconductance	$g_{fs}$	$I_D = -1\text{ mA}, f = 1\text{ kHz}$	6	-	920	-	$\mu\text{mho}$
Low-Frequency Noise Voltage	$e_N$	$I_D = -1\text{ mA}, f = 1\text{ kHz}, R_s = 0\text{ }\Omega$	7	-	0.03	-	$\mu\text{V } \sqrt{\text{Hz}}$
Low-Frequency Noise Current	$i_N$	$I_D = -1\text{ mA}, f = 1\text{ kHz}, R_s = 1\text{ M}\Omega$	7	-	0.2	-	$\rho\text{A } \sqrt{\text{Hz}}$
Current-Mirror Transfer Ratio ( $p_1/p_2$ )	$I_{MTR}$	$I_1 = -100\text{ }\mu\text{A}, V_{DS} = -10\text{ V}$	30	0.7	1.1	1.5	-
Gate-Terminal Current	$I_{GT}$	$V_{DS} = -10\text{ V}, V_{GS} = -3.5\text{ V}$	-	-	$\pm 0.015$	-40	nA
Input Capacitance	$C_I$	-	-	-	6.3	-	pF
Output Capacitance	$C_O$	-	-	-	3	-	pF
Input-to-Output Capacitance	$C_{I-O}$	-	-	-	0.75	-	pF
<b>For Each n-Channel MOS Transistor</b>							
Drain Current	$I_D$	$V_{DS} = +10\text{ V}, V_{GS} = +3.6\text{ V}$	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	$I_D = 10\text{ }\mu\text{A}$	-	-	1.5	-	V
Gate-to-Source Voltage Differential ( $n_1$ vs $n_2$ )	$ V_{GS1} - V_{GS2} $	$I_D = 100\text{ }\mu\text{A}, V_{DS} = +10\text{ V}$	5	-	$\pm 30$	-	mV
Forward Transconductance	$g_{fs}$	$I_D = 1\text{ mA}, f = 1\text{ kHz}$	6	-	860	-	$\mu\text{mho}$
Low-Frequency Noise Voltage	$e_N$	$I_D = 1\text{ mA}, f = 1\text{ kHz}, R_s = 0\text{ }\Omega$	7	-	0.2	-	$\mu\text{V } \sqrt{\text{Hz}}$
Low-Frequency Noise Current	$i_N$	$I_D = 1\text{ mA}, f = 1\text{ kHz}, R_s = 1\text{ M}\Omega$	7	-	0.3	-	$\rho\text{A } \sqrt{\text{Hz}}$
Current-Mirror Transfer Ratio ( $n_1/n_2$ )	$I_{MTR}$	$I_1 = 100\text{ }\mu\text{A}, V_{DS} = +10\text{ V}$	29	0.7	1.3	2.0	-
Gate-Terminal Current	$I_{GT}$	$V_{DS} = +10\text{ V}, V_{GS} = +3.7\text{ V}$	-	-	$\pm 0.01$	+40	nA
Input Capacitance	$C_I$	-	-	-	5.5	-	pF
Output Capacitance	$C_O$	-	-	-	2.0	-	pF
Input-to-Output Capacitance	$C_{I-O}$	-	-	-	0.35	-	pF
<b>For Each CMOS Transistor Pair</b>							
Drain Current	$I_{DD}$	$V_{DD} = +10\text{ V}$	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	$V_{DD} = +10\text{ V}, V_{SS} = 0\text{ V}$ Gate Voltage ( $V_G$ ) = +10 V or 0 V	8	-	0.5	100	nA
DC Output Voltage	$V_O$	$V_{DD} = +10\text{ V}$	10	4.2	5.0	5.8	V
Forward Transconductance	$g_{fs}$	$V_{DD} = +10\text{ V}, f = 1\text{ kHz}$	6	-	2300	-	$\mu\text{mho}$
Slew Rate (Open-Loop)	SR	$V_{DD} = +15\text{ V}$	10	-	95	-	$\text{V } \mu\text{s}$
Amplifier Voltage Gain	$A_{OL}$	$V_{DD} = +10\text{ V}, f = 1\text{ kHz}, R_b = 22\text{ M}\Omega$ $R_s = 50\text{ }\Omega$	10,11	-	32	-	dB
Gate-Terminal Current	$I_{GT}$	$V_{DD} = +10\text{ V}$	10	-	$\pm 0.005$	$\pm 20$	nA
Broadband Output Noise Voltage	$E_{ON}$	$V_{DD} = +10\text{ V}, R_b = 22\text{ M}\Omega, R_s = 10\text{ k}\Omega$	10,11	-	500	-	$\mu\text{V}$
Input Capacitance	$C_I$	-	-	-	11.8	-	pF
Output Capacitance	$C_O$	-	-	-	5.0	-	pF
Input-to-Output Capacitance	$C_{I-O}$	-	-	-	1.1	-	pF

# CA3600

## TYPICAL CHARACTERISTICS CURVES

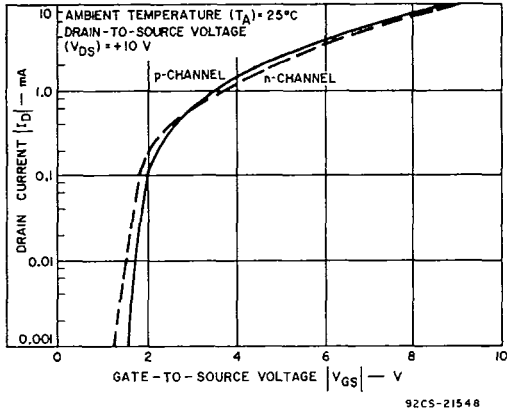


Fig. 2—Drain current vs. gate-to-source voltage.

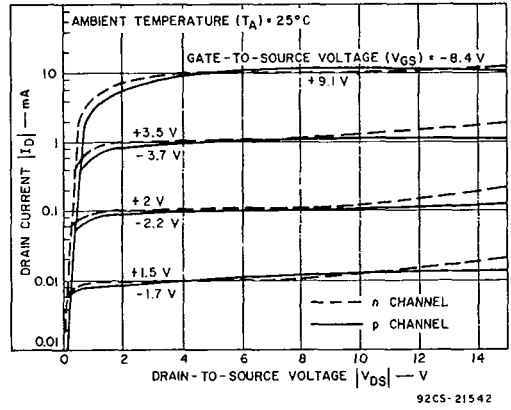


Fig. 3—Drain current vs. drain-to-source voltage.

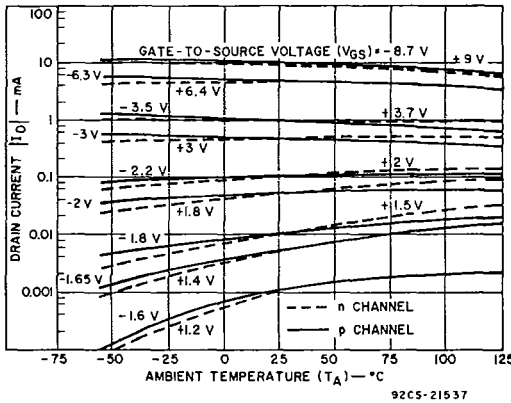


Fig. 4—Drain current vs. ambient temperature.

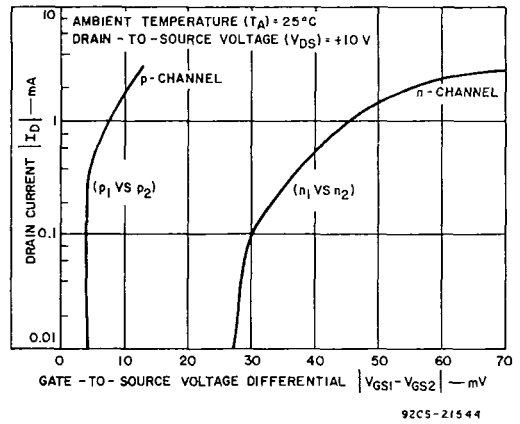


Fig. 5—Gate-to-source voltage differential vs. drain current.

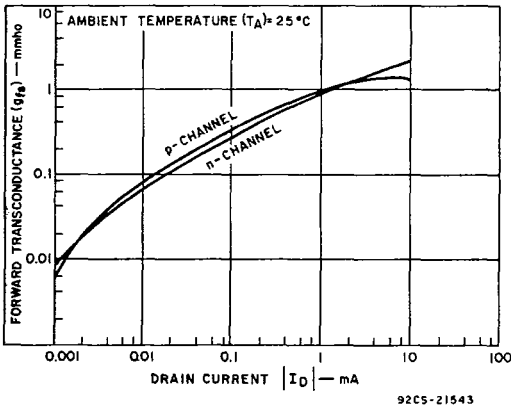


Fig. 6—Forward transconductance vs. drain current.

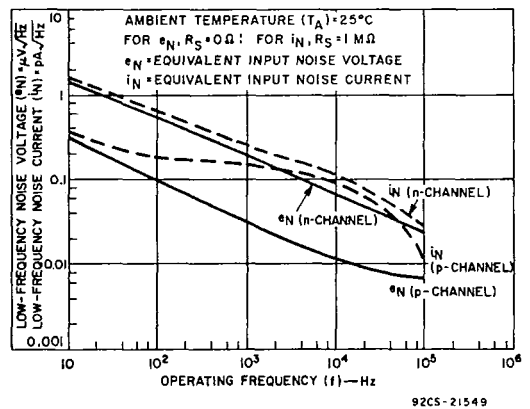


Fig. 7—Noise voltage and noise current vs. operating frequency.

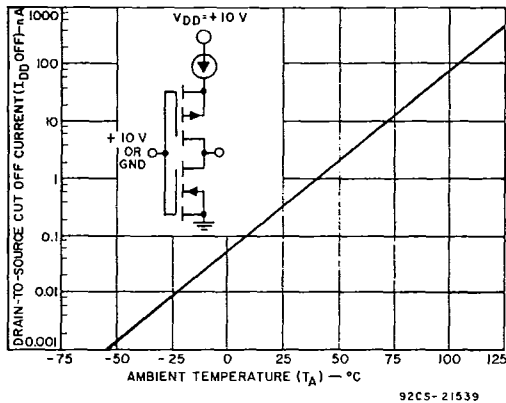


Fig. 8— Drain-to-source cutoff current vs. ambient temperature.

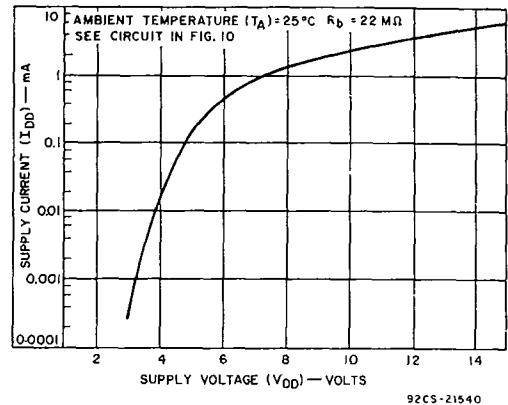


Fig. 9— Typical  $V_{DD}$  vs.  $I_{DD}$  characteristics for amplifier circuits of Fig. 10 and Fig. 15.

## APPLICATIONS

### The Basic CMOS Linear Amplifier

P-n-p and n-p-n bipolar transistors have been used for many years in the design of so-called "true-complementary" linear amplifier circuits<sup>1</sup>. Since mutually compatible p-channel and n-channel MOS FET devices were not generally available, "true-complementary" amplifier circuits using MOS transistors were seldom used. Now, CMOS transistor technology<sup>5</sup> has made it possible to supply compatible p-channel/n-channel transistors in monolithic IC form such as the CA3600E CMOS transistor array shown in Fig. 1.

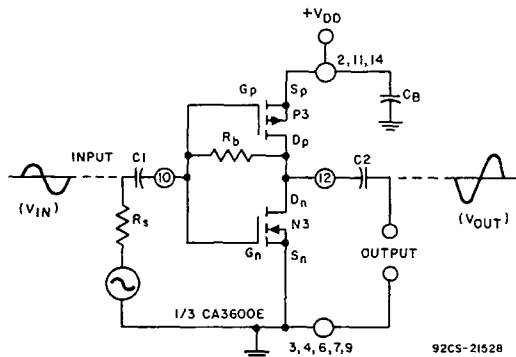


Fig. 10— CMOS transistor-pair biased for linear-mode operation.

### A "True-Complementary" Linear Amplifier Using CMOS Transistors

Fig. 10 shows the schematic diagram of a single-stage "true-complementary" linear amplifier using one pair of the complementary MOS transistors in the CA3600E, connected in a common-source circuit. Resistor  $R_b$  is used to bias the complementary pair for Class A operation, as described subsequently, and  $R_s$  represents the source resistance of the

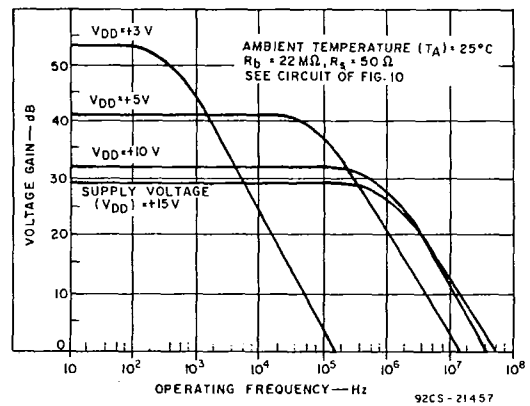


Fig. 11— Typical voltage gain vs. frequency characteristics for amplifier circuit of Fig. 10.

signal source. This generic amplifier is suitable for operation with a single or split voltage supply in the range of 3 to 15 volts. Fig. 11 shows voltage gain as a function of operating frequency at various supply voltages for the single-stage amplifier. This amplifier is capable of producing very high output-swing voltages ( $V_{OUT}$ ); for example, its output voltages can be swung to within several millivolts of either supply-voltage "rail". Fig. 9 shows typical supply voltage ( $V_{DD}$ ) vs. supply current ( $I_{DD}$ ) characteristics for the single-stage amplifier. The curves in Fig. 12 show the normalized amplifier supply current as a function of ambient temperature at various supply voltages. When the amplifier is operating at  $V_{DD} = 3$  V, the supply current changes rapidly as a function of temperature because the MOS transistors are operating in the proximity of their individual gate-source threshold voltages.

# CA3600

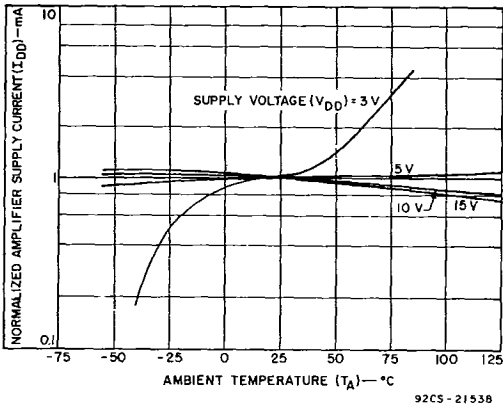


Fig. 12— Normalized amplifier supply current vs. ambient temperature characteristics for amplifier circuit of Fig. 10.

## Voltage-Transfer Characteristics

Fig. 13 illustrates a voltage-transfer characteristic curve of a CMOS transistor pair connected in the amplifier circuit of Fig. 10, with a biasing resistor ( $R_b$ ) connected between the drain and gate terminals (10,12). If the p- and n-channel transistors have identical characteristics, their channel resistances are equal, and the biasing method shown establishes a steady-

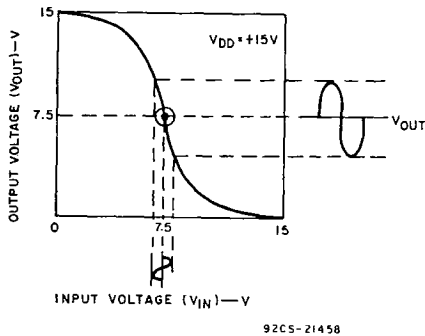


Fig. 13— Representation of voltage-transfer characteristics for CMOS transistor pair.

state condition such that terminal 12 is at mid-potential between  $V_{DD}$  and ground. Thus, with negligibly small gate-source leakage resistances, under zero-signal conditions, the biasing resistor ( $R_b$ ) establishes gate potential at the mid-point between  $V_{DD}$  and ground, i.e.,  $V_{IN} = V_{OUT}$ . Under these conditions the amplifier is biased for operation about the mid-point ("0") in the linear segment on the steep transition of the voltage-transfer characteristic as shown in Fig. 13. When the input signal ( $V_{IN}$ ) swings in the positive direction, there is a reduction in the instantaneous output voltage ( $V_{OUT}$ ) with respect to ground. Negative-going input signals have inverse effects. Thus, phase-inversion occurs in the CMOS-pair amplifier. Power-supply current is constant during dynamic

linear operation, i.e., Class A amplifier service. When the signal input-voltage level ( $V_{IN}$ ) becomes very large, the output signal ( $V_{OUT}$ ) waveforms become distorted because the transistors are driven into the non-linear portions of their voltage-transfer characteristics. If the positive-going input-signal is sufficiently large, for example, the p-channel transistor can be driven to cutoff and the amplifier supply current ( $I_{DD}$ ) is reduced to essentially zero.

Fig. 14 shows typical voltage-transfer characteristics of each CMOS pair in the CA3600E at several values of  $V_{DD}$ . The shape of these transfer characteristics is comparatively constant despite temperature changes from  $-55$  to  $+125^{\circ}C$ .

The biasing arrangement used in the circuit of Fig. 10 provides an easy method of establishing feedback for ac signals in accordance with the  $R_b/R_s$  ratio. When the feedback of ac signals is not desirable, the circuit of Fig. 15 may be used. The ac bypass capacitor ( $C_3$ ) minimizes ac signal feedback.

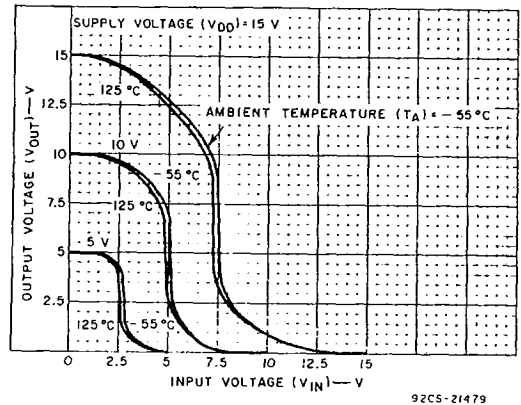


Fig. 14— Voltage transfer characteristics for CMOS transistor-pair amplifier in Fig. 10.

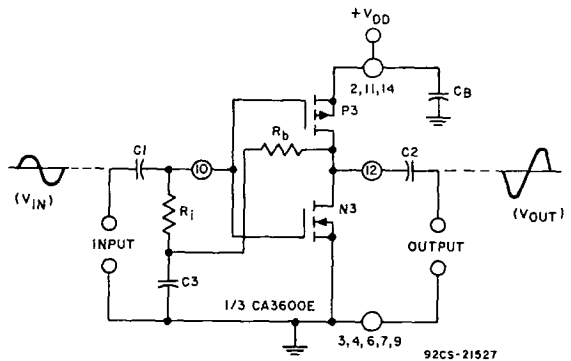


Fig. 15— Alternate method of biasing CMOS transistor-pair for linear-mode operation.

## Cascading Amplifier Stages of CMOS Transistor Pairs

Ultra-high-gain amplifiers can be designed by cascading stages of CMOS transistor pairs as shown in Fig. 16. The biasing system used is similar to that described above in connection with Fig. 10. The supply current for the three-stage amplifier shown in Fig. 16 is typically three times the values shown in Fig. 9. Gain and frequency-response characteristics of the amplifier are shown in Fig. 17.

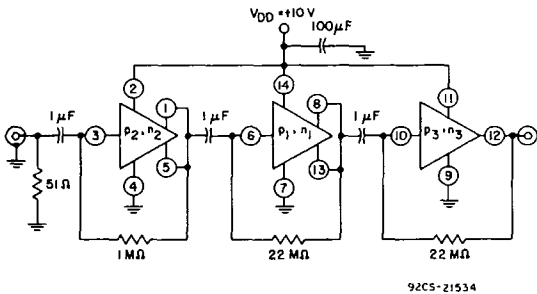


Fig. 16— High-gain amplifier uses cascaded CMOS transistor-pair in CA3600E.

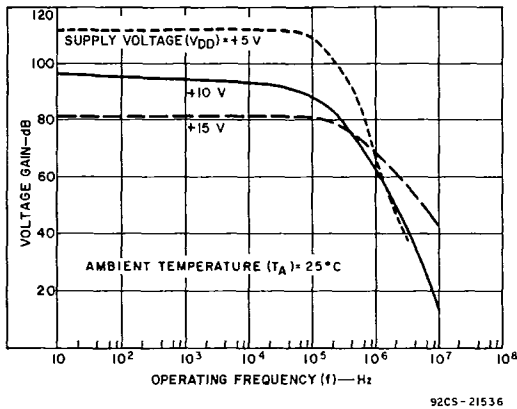


Fig. 17— Typical voltage gain vs. operating frequency characteristics for three-stage CMOS transistor-pair amplifier in Fig. 16.

## Post-Amplifiers For Op-Amps

CMOS transistor-pairs can be advantageously applied as post-amplifiers for op-amps. Because the input impedance of the CMOS pair is comparatively high, the op-amp operates under essentially unloaded conditions. Each CMOS pair can sink and source output current up to about 10 mA. Additionally, the op-amp output can be directly coupled to bias the CMOS pair. A detailed description of the subject has been published previously.<sup>2</sup>

The schematic diagram in Fig. 18 shows a CMOS transistor-pair serving as a post-amplifier to an RCA-CA3080 Operational Transconductance Amplifier.<sup>3</sup> The approximate 30-dB

gain in a single CMOS transistor-pair is an added increment to the 100-dB gain in the CA3080, yielding a total forward gain of about 130 dB. The open-loop slew rate of the circuit in Fig. 19 is approximately 65 V/ $\mu$ s. When compensated for the unity-gain voltage-follower mode shown in Fig. 19, the slew rate is about 1 V/ $\mu$ s. For greater current output, the two remaining transistor pairs of the CA3600E may be connected in parallel with the single stages shown in Figs. 18 and 19. The use of the two-stage CMOS post-amplifier shown in Fig. 20 increases the total open-loop gain of the system to about 160 dB (100,000,000X). Open-loop slew rate remains at about 65 V/ $\mu$ s. A slew rate of about 1 V/ $\mu$ s is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 21. These circuits operate in concert with stability.

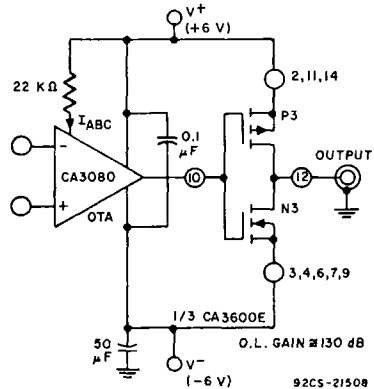


Fig. 18— CMOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

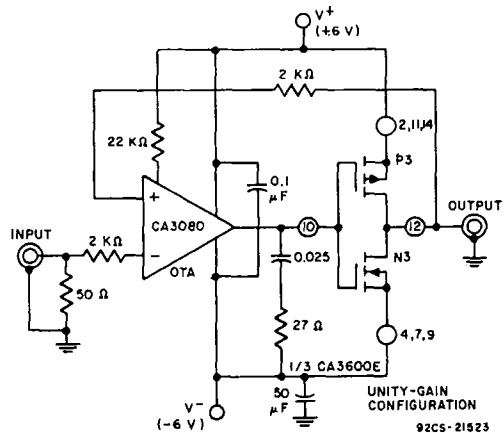


Fig. 19— CMOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

# CA3600

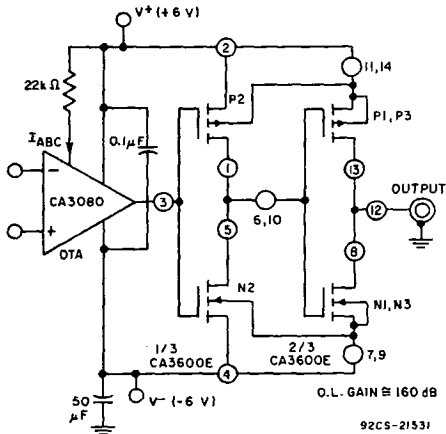


Fig. 20— CMOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.

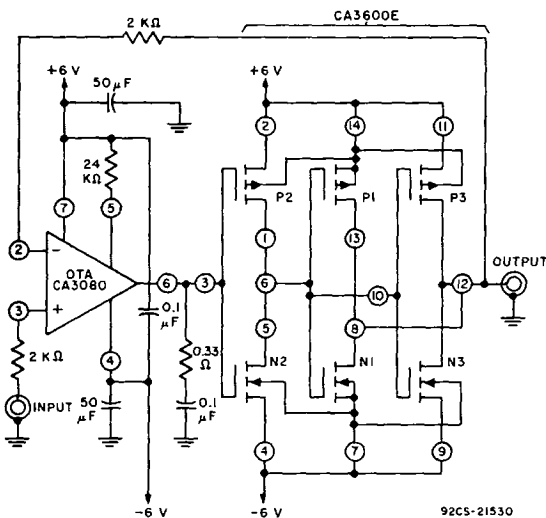
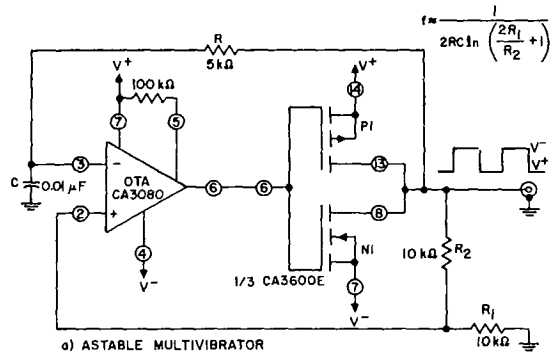


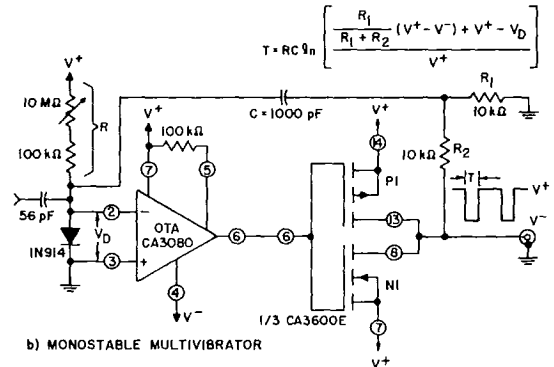
Fig. 21— Unity-gain amplifier uses CMOS transistor-pairs as two-stage post-amplifier to op-amp.

## Multivibrators, Threshold Detectors, and Comparators

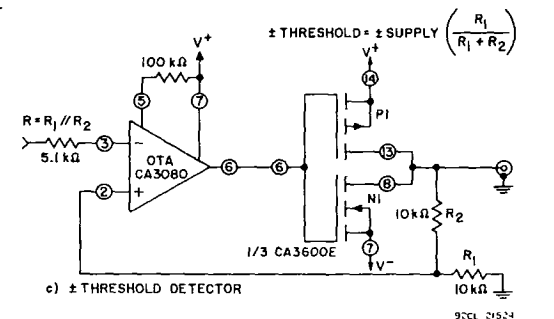
Descriptions of several circuits using CMOS transistor-pairs in both monostable and astable multivibrators have been published.<sup>4,5</sup> The characteristics of CMOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier.<sup>2,3</sup> Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current ( $I_{ABC}$ ) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.



a) ASTABLE MULTIVIBRATOR



b) MONOSTABLE MULTIVIBRATOR



c) ± THRESHOLD DETECTOR

Fig. 22— Multistable circuits using CMOS transistor-pairs.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and CMOS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW (typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is -1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB.



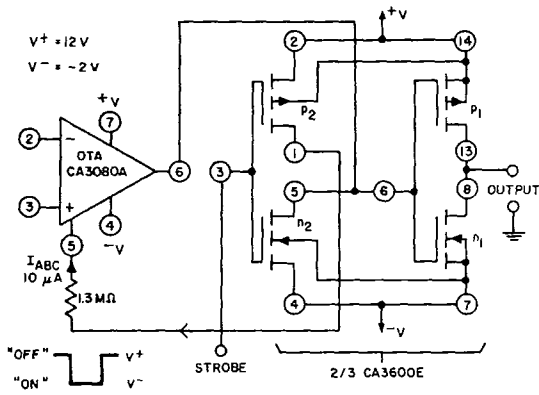


Fig. 23— Programmable micropower comparator.

### Operational Amplifiers

CMOS transistor-pairs can be used in conjunction with a bipolar transistor-array IC to build an op-amp as shown in Fig. 24. It is particularly suited for single-supply operation (e.g., mobile and aircraft service). The op-amp is unique in that it is responsive to small-signal ground-referenced inputs and the output stage can easily be driven within 1 mV of ground potential. Its open-loop gain characteristics are shown in Fig. 25; the open-loop slew rate is approximately 30 V/μs.

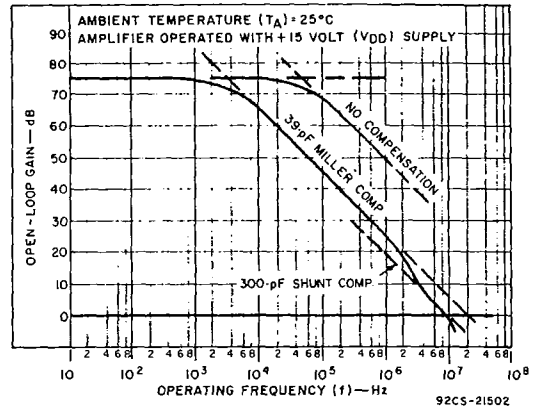


Fig. 25— Open-loop gain characteristic for op-amp in Fig. 24.

This circuit is ideal for use as a unity-gain voltage-follower and has been described for operation in connection with a 9-Bit Single-Supply Digital-to-Analog Converter (DAC) using CMOS transistors in the resistor-network switches.<sup>6</sup>

The op-amp in Fig. 24 has three stages; its first stage is a differential input circuit using two p-channel transistors (P<sub>4</sub>, P<sub>5</sub>) in a CA3600E. The second stage is an n-p-n

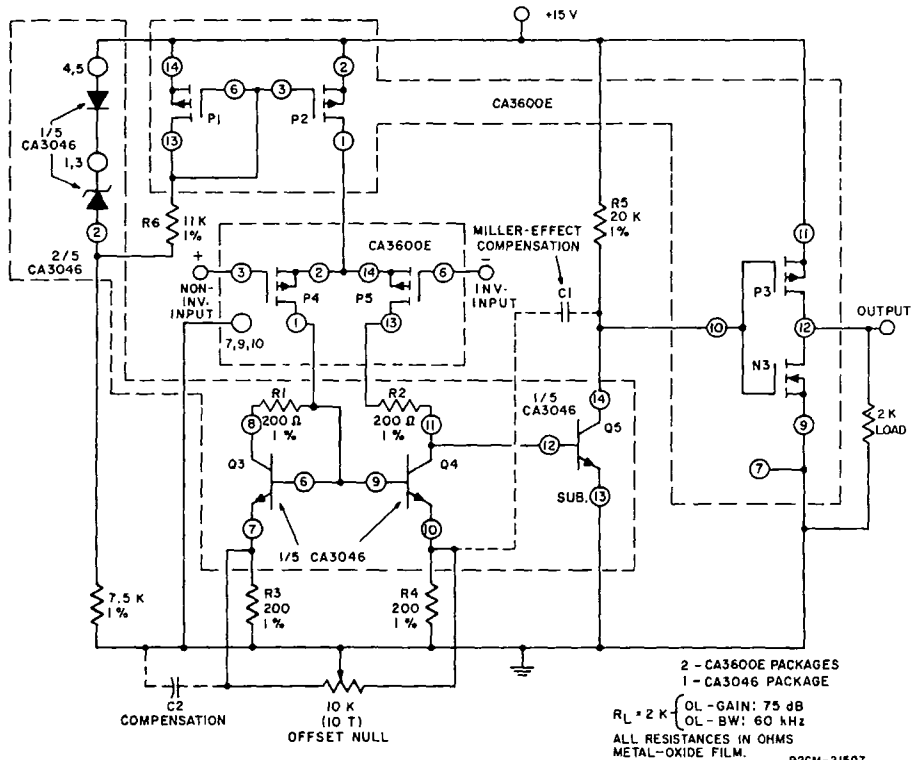


Fig. 24— Operational amplifier using CMOS transistor-pairs.

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transistor ( $Q_5$ ) and the output stage is a CMOS transistor-pair ( $P_3, N_3$ ) operating in the manner described above. A constant current of about  $400 \mu\text{A}$  is established in the differential input stage by the zener network in the upper-left portion of Fig. 24. The zener network energizes a current mirror comprised of two p-channel transistors ( $P_1, P_2$ ) to establish constant-current flow in the differential amplifier stage ( $P_4, P_5$ ). The drain load for the differential amplifier consists of resistors  $R_1, R_4$  and a current mirror ( $Q_3, Q_4$ ) to optimize conditions for balanced operation of the differential amplifier. The operating theory of current-mirror circuits has been described in reference.<sup>2</sup> Amplifier voltage-offset is nulled with the 10-kilohm balance potentiometer. The second-stage current is established by  $R_5$ , and is selected to approximate the first-stage current level ( $400 \mu\text{A}$ ), to assure similar positive and negative slew rates. The amplifier is shown driving a 2-kilohm load, a typical value used with monolithic op-amps. Voltage gain varies inversely with the choice of load resistance.

The amplifier can be compensated with a single capacitor ( $C_1$ ), connected as shown by the dotted lines. However, optimum compensation for the unity-gain non-inverting mode is provided by two capacitors: Miller Effect feedback through a 39-pF capacitor  $C_1$  (connected as shown), and a 300-pF capacitor connected between terminals 7 and 13 of the CA3046 transistor array to shunt one-half the driving current. Fig. 25 shows the open-loop gain characteristics with compensation for unity-gain operation. When the amplifier is operated as a voltage-follower, it is recommended that a 1-kilohm resistor, shunted with a 150-pF capacitor, be connected between the amplifier output terminal and terminal 6 of  $P_5$  to avoid a potential latch situation involving the integral gate-protection network. The circuit can also be latched if either input terminal is driven more than about 0.7 volt below ground potential. This latch situation can be avoided by connecting a 1N914 diode from each input terminal to ground, with the diode anode grounded.

### Analog Timer

The CA3600E is useful in the design of analog timer circuits. A typical circuit is shown in Fig. 26. For purposes of explanation, let it be assumed that capacitor  $C_1$  initially is in a completely discharged condition; terminal 10, therefore, is initially at ground potential and transistor  $N_3$  is non-conductive. The circuitry at the left of terminal 10 provides a source of constant-current flow through  $P_1$  to charge capacitor  $C_1$  increasingly positive with respect to ground. After the passage of time ( $T$ ), capacitor  $C_1$  is charged sufficiently in the positive direction so that transistor  $N_3$  is driven into conduction by its gate and the lamp is lighted to signify the end of the time-delay period. The circuit is reset by momentarily closing switch  $S_1$  to discharge capacitor  $C_1$  through  $R_4$ . Resistor-divider network  $R_1, R_2$  establishes the supply voltage to a constant-current network comprised of resistor  $R_3$  and the series-connected COS/MOS pair  $N_2, P_2$ , biased for linear operation by resistor  $R_5$  as previously described. This combination is connected to the gate terminal (No. 6) of

transistor  $P_1$  to form a current mirror, i.e., the current flowing through  $P_1$  to charge  $C_1$  will be essentially equal to the constant-current flow established through  $R_3, N_2$ , and  $P_2$ . A description of current-mirror operation with MOS transistors is given subsequently.

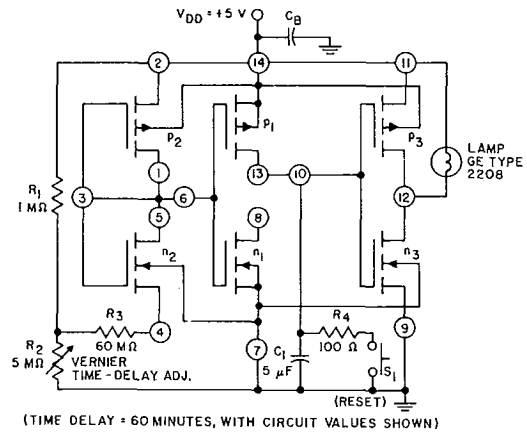


Fig. 26—Analog timer using CA3600E.

### Oscillator Circuits

Oscillator circuits using CMOS transistor-pairs have been widely used for several years in clock and watch circuits because of their low power consumption and good frequency stability. Details of their operating theory and characteristics have been published.<sup>5,7</sup>

The design of CMOS oscillator circuits, like the design of any oscillator circuit, involves the provision of an amplifying section to operate compatibly with an appropriate feedback network. A single-stage amplifier using a CMOS transistor-pair has already been described. A suitable feedback network to insure stable oscillator performance is easily added, as illustrated in connection with the crystal oscillator circuit shown in Fig. 27. The familiar pi-network has been connected between the input and output terminals, points "D" and "G", to provide the required  $180^\circ$  phase shift for stable oscillator performance. The frequency-determining crystal is an integral part of the pi-network feedback circuit. The resistors  $R_1$  and  $R_2$  decrease the total power consumption of the oscillator at a particular supply voltage and enhance the frequency stability. Variable frequency oscillators can be built by replacing the crystal with an appropriate inductance and tuning the pi-network by conventional means.

### Current Mirrors Using MOS Transistors

Monolithic linear IC's using bipolar transistors frequently employ so-called "current-mirror" circuits. The theory and practical applications of current mirrors using bipolar transistors have been described in the literature.<sup>2</sup> As shown in

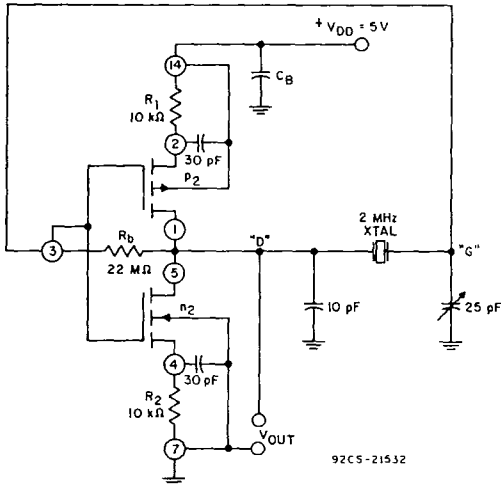


Fig. 27— Typical crystal-oscillator circuit using CMOS transistor-pair (1/3 CA3600E).

Fig. 28, a rudimentary form of "current-mirror" consists of a transistor  $Q_1$  with a second transistor  $Q_2$  connected as a diode. When both transistors have identical characteristics, a current  $I_1$  forced to flow through  $Q_2$  produces a current ( $I_2$ ) of equal magnitude to flow in the collector of  $Q_1$  (provided there is sufficient collector potential for  $Q_1$ ). In a common form of application, a source of potential is used to force

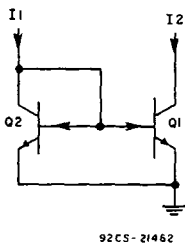


Fig. 28— Current mirror using n-p-n bipolar transistors.

constant-current flow  $I_1$ , and thus to establish the flow of constant current  $I_2$  through  $Q_1$ . Arrangements of this generic current-mirror type are frequently used when  $Q_1$  acts as the common-emitter impedance in a differential-amplifier circuit.

MOS transistors are also applicable as current mirrors, as shown in Fig. 29. The diode-connected MOS transistor  $N_2$  functions as a transistor with 100 per-cent feedback. Therefore, the gate-to-source voltage ( $V_{GS}$ ) in  $N_2$  retains control of the drain current as in normal transistor action, i.e.,  $I_D \cong g_{fs} V_{GS}$ , where  $g_{fs}$  is the forward transconductance of the device. If a current  $I_1$  is forced into the diode-connected transistor ( $N_2$ ), the gate-to-source voltage will rise until equilibrium is reached. Thus, a gate-to-source voltage is established in  $N_2$  such that  $N_2$  "sinks" the applied current  $I_1$ .

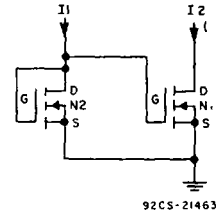


Fig. 29— Current mirror using n-channel MOS transistors.

If the gate and source terminals of another transistor ( $N_1$ ) are connected in shunt with the gate and source terminals of  $N_2$ , as shown in Fig. 29,  $N_1$  is also able to "sink" a mirror current approximately equal to that flowing in the drain lead of the diode-connected transistor  $N_2$ . It is assumed that both MOS transistors have identical characteristics, a prerequisite that is essentially established by the monolithic IC fabrication technology used in manufacturing the CA3600E CMOS transistor array.

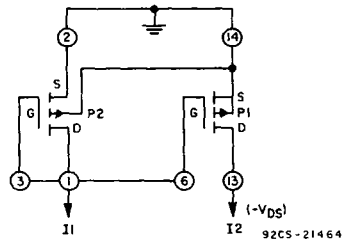


Fig. 30— Current mirror using p-channel MOS transistors in CA3600E.

Current mirrors can also be designed with p-channel MOS transistors as illustrated by the arrangement in Fig. 30 using transistors in the CA3600E. The characteristics of a current mirror using the p-channel transistors in the CA3600E are superior to those which can be achieved with a current mirror using the n-channel transistors because the characteristics of the p-channel transistors are more nearly matched. The data

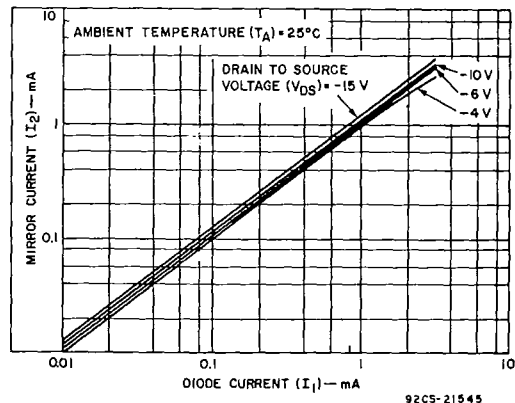


Fig. 31— Characteristics of current mirror circuit of Fig. 30 using p-channel transistors.

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contained in Fig. 31 show the high degree of tracking between  $I_1$  and  $I_2$  for several values of drain voltage  $V_D$ . Fig. 32 also illustrates the fact that this high degree of tracking between  $I_1$  and  $I_2$  can be maintained to within about one per-cent despite wide variations in ambient temperature.

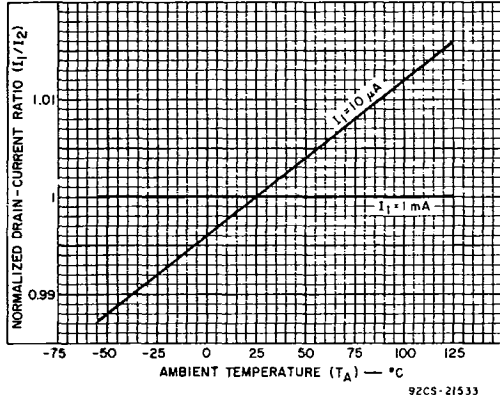


Fig. 32—Normalized drain current ratio vs. ambient temperature for typical current mirror using p-channel transistors (Fig. 30).

The op-amp circuit in Fig. 24 contains an illustrative example of a current-mirror circuit using two p-channel transistors in the CA3600E. Transistor  $P_2$  serves as a constant-current source ( $\cong 400 \mu A$ ) for the differential amplifier, consisting of transistors  $P_4$  and  $P_5$  and their drain-load network. Transistor  $P_2$  is in a "mirrored" connection with transistor  $P_1$ . A stabilized source of supply potential is developed across the zener diode (terminals 11 and 12 of the CA3083) and drives about  $400 \mu A$  of current through  $R_6$  and  $P_1$ .

### Complementary Current Mirrors Using CMOS Transistor-Pairs

CMOS transistor-pairs can be applied advantageously in the design of Complementary Current-Mirrors, as shown in Fig. 33. Transistors  $P_1$  and  $N_1$  are series-connected and biased for linear operation as previously described, so that there is a current flow  $I_{D1}$  through  $P_1$  and  $N_1$ . The potential developed between terminals 13 and 14 is applied as gate-source (2,3) voltage for  $P_2$ , forcing "mirror" operation of  $P_2$  to produce a current source  $I_{D2-p}$  equal to  $I_{D1}$ . Likewise, the potential developed between terminals 7 and 8 is applied as gate-source (3,4) voltage for  $N_2$  forcing "mirror" operation of  $N_2$  to produce a current-sink  $I_{D2-n}$  equal to  $I_{D1}$ .

A variant of this complementary current mirror is used in the analog timer circuit shown in Fig. 26. Transistors  $P_2$  and  $N_2$  are series-connected together with a 60-megohm resistor to establish their drain current at 5 nA. The potential developed across terminals 1 and 2 also appears as the gate-source voltage for transistor  $P_1$ , thereby establishing a mirror-current source of 5 nA at terminal 13 to charge capacitor  $C_1$  linearly. In this circuit, the "mirrored" current-sink available at terminal 8 (transistor  $N_1$ ) is unused. This type of current-mirror configuration is exceptionally stable with temperature variations.

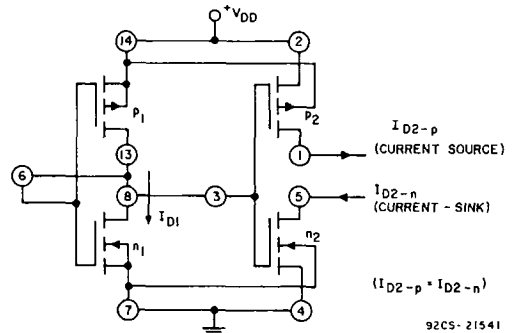


Fig. 33—Complementary current mirrors using CMOS transistor-pairs in CA3600E.

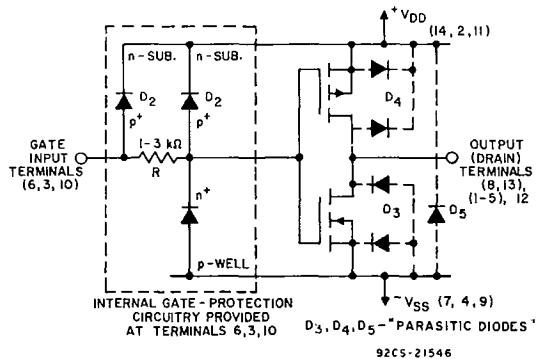


Fig. 34—Integral protection circuits used in CA3600E.

### Considerations in Handling CA3600E Devices

Failure of the gate-channel oxide was a persistent problem in early MOS devices. The breakdown of the oxide is generally in the order of 100 volts, and the dc resistance is in the order of  $10^{12}$  ohms. Because of this extremely high resistance, even a very-low-energy source (such as static charge) is capable of developing sufficient voltage to cause damage. Furthermore, the oxide can be punctured and damaged by a single voltage excursion beyond the breakdown limit.

Fig. 34 shows a protection circuit<sup>5,8</sup> which is incorporated at each gate-lead of the CA3600E. A typical value of 1 to 3 kilohms is used for the input resistor  $R_1$ , which functions in combination with the capacitance of the gate and the associated protective diode to integrate and clamp input voltages to a safe level. This circuit also shows the "substrate diodes" ( $D_3$ ,  $D_4$ , and  $D_5$ ) which provide protection to the MOS channels at the output terminals.

Although the gate-protection system is very effective in guarding against damage due to static charges, it is prudent to observe the following precautions:<sup>5,9</sup>

1. The leads of devices should be in contact with a conductive material, except when being tested or in actual operation. A conductive material such as "ECCOSORB LD26"<sup>\*</sup> or equivalent is suggested for use during storage and/or handling. Devices should not be inserted in non-conductive containers such as conventional plastic "snow" or trays.
2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals from low-impedance sources should not be applied to the gate terminals while the power supply is off. As a corollary, it follows that the power supply

should not be turned off while a signal from a low-impedance source is being applied to any gate terminal. When the  $V_{DD}$  supply is off, the positive "back-bias" voltage is removed from the cathode of diode  $D_2$  (see Fig. 34). Consequently, an input signal with positive-going polarity can drive  $D_2$  into conduction. Under these conditions a low-impedance signal source can provide sufficient current to permanently damage  $D_2$  and/or melt aluminum interconnection paths. Therefore, if, in any system design using the CA3600E, any gate input excursion is expected to exceed  $+V_{DD}$  or fall below  $-V_{SS}$ , the current through the input diodes should be limited to  $100 \mu\text{A}$ .

5. All unused gate-input terminals should be connected to  $V_{SS}$  (ground). When source terminals (e.g., Nos. 2 and 11) of p-channel transistors are unused in circuitry, they should be connected to terminal No. 14. Likewise, when source terminals (e.g., Nos. 4 and 9) of n-channel transistors are unused, they should be connected to terminal No. 7.
6. After CA3600E units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system, the board is no more than an extension of the device leads mounted on the board. It is a good practice to place conductive tape or jumpers on circuit-board terminals to "ground" gate terminals.
7. In some applications of the CA3600E separate positive and negative power supplies may be employed (e.g., see Fig. 22). In such applications provisions must be made so that the positive supply voltage is applied prior to the application of negative supply voltage and vice versa on shutdown. This precaution is necessary to avoid possible damage due to "latching" involving the substrate and protective diode circuits.

<sup>\*</sup> Trade Mark: Emerson and Cumming, Inc.